

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	doubled near4 sided near4 capacitor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 13:51
L2	12614	double near4 capacitor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 13:51
L3	323285	second near (conductive or conductor or conducting or metal or upper or higher or electrode)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 13:52
L4	5625775	(plug contact interconnect interconnection interconnected interconnecting (via adj hole))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 13:53
L5	1008	2 and 3 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 13:53
L6	268	5 and spacer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 13:54
L7	235	6 and ((@ad<"20030728") or (@rlad<"20030728"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:55
L8	781	(first adj conductive near4 spacer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:41

## EAST Search History

L9	293	8 and capacitor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:41
L10	31816	Micron.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:41
L11	30	9 and 10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:44
L12	6503	(trench near capacitor)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:45
L13	641	12 and 10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:45
L14	520	13 and dielectric	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:45
L15	107	14 and ((top or upper) near plate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:50
L16	851	(438/243).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/04/05 15:29

## EAST Search History

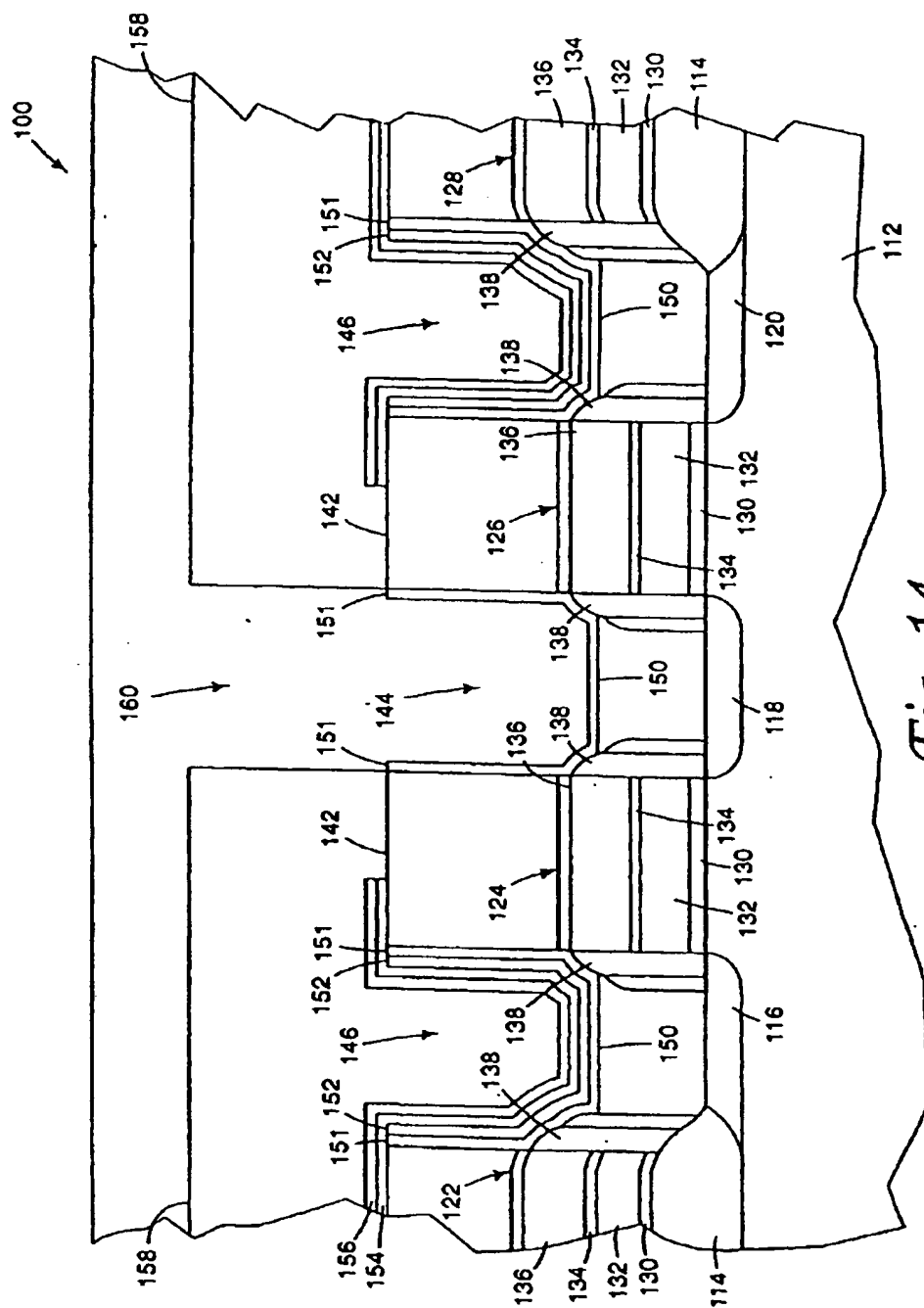
L17	479	(438/244).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/04/05 15:50
L18	439	(438/250).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/04/05 16:06
L19	614	(438/254).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/04/05 14:50
L20	2161	16 or 17 or 18 or 19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:51
L21	1324	(second near (conductive conductor conducting metal) near4 spacer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:52
L22	45	20 and 21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:52
L23	31816	Micron.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:50
L24	363	(opening trench hole) near8 (conductive near spacer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:51

## EAST Search History

L25	24	23 and 24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:52
L26	454	Graettinger.in. or Pontoh.in. or Figura.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:52
L27	5	24 and 26	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:53
L28	315595	(second near (conductive conducting conductor metal upper electrode bottom))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:53
L29	810473	(second near4 (conductive conducting conductor metal upper electrode bottom))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:53
L30	270567	(second near4 (dielectric insulator insulating cell insulated))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:54
L31	120871	29 and 30	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:54
L32	83	26 and 31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:54

## EAST Search History

L33	71	32 and ((@ad<"20030728") or (@rlad<"20030728"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:56
L34	2932	((second near4 dielectric) same (second near4 (conductive conductor metal electrode upper top bottom lower conducting)) same capacitor).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:58
L35	693315	(plug or contact).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:58
L36	1432	34 and 35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:59
L37	1609592	(opening via hole through-hole open groove vertical).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 16:00
L38	919	36 and 37	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 16:01
L39	69784	spacer.clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 16:01
L40	126	38 and 39	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/05 16:01

*Fig. 14*



US006737696B1

(12) **United States Patent**  
**DeBoer et al.**

(10) **Patent No.:** **US 6,737,696 B1**  
(45) **Date of Patent:** **\*May 18, 2004**

(54) **DRAM CAPACITOR FORMULATION USING  
A DOUBLE-SIDED ELECTRODE**

(75) **Inventors:** **Scott J. DeBoer**, Boise, ID (US);  
**Husam Al-Shareef**, Boise, ID (US);  
**Randhir Thakur**, Cupertino, CA (US)

(73) **Assignee:** **Micron Technology, Inc.**, Boise, ID  
(US)

(\*) **Notice:** This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** **09/089,445**

(22) **Filed:** **Jun. 3, 1998**

(51) **Int. Cl.<sup>7</sup>** ..... **H01L 27/108; H01L 29/76;**  
**H01L 29/94; H01L 31/119**

(52) **U.S. Cl.** ..... **257/306; 257/309**

(58) **Field of Search** ..... **257/295-313,**  
**257/532-535; 438/243-255, 396-399**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,278,091 A 1/1994 Fazan et al.

5,340,765 A 8/1994 Dennison et al.  
5,362,632 A 11/1994 Matthews  
5,612,574 A \* 3/1997 Summerfelt et al. .... 257/295  
5,627,094 A 5/1997 Chan et al.  
5,741,722 A \* 4/1998 Lee ..... 438/396  
5,786,250 A \* 7/1998 Wu et al. .... 438/254  
5,817,555 A \* 10/1998 Cho ..... 438/253  
5,960,294 A \* 9/1999 Zahurak et al. .... 438/398  
5,973,351 A \* 10/1999 Kotecki et al. .... 257/310

\* cited by examiner

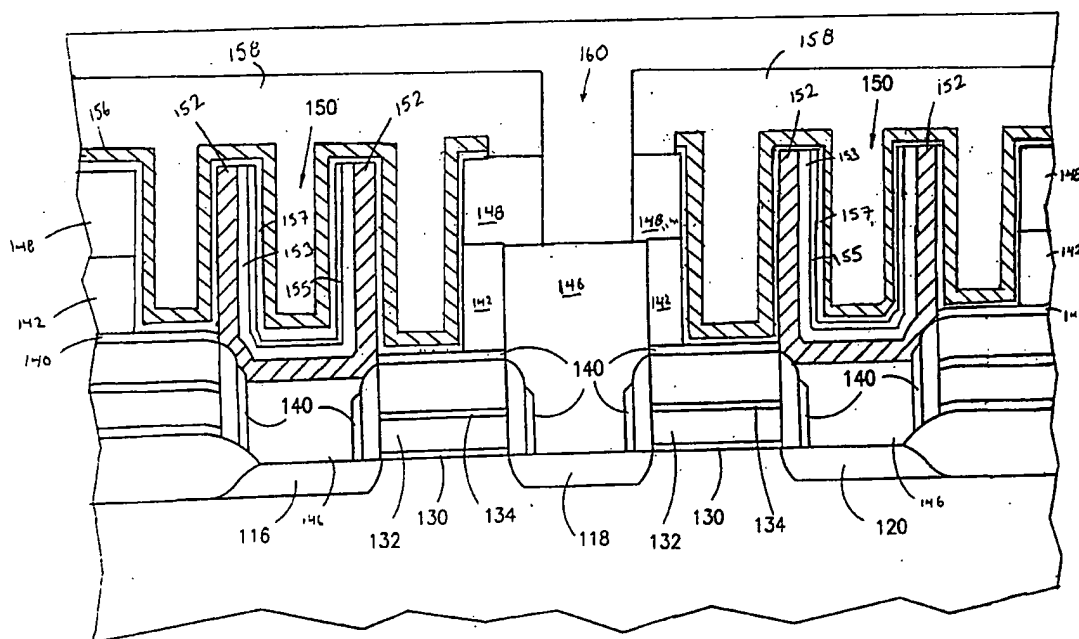
*Primary Examiner*—Cuong Nguyen

(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin & Oshinsky LLP

(57) **ABSTRACT**

A capacitor having a double sided electrode for enhanced capacitance. In one embodiment, the double sided electrode capacitor is a stacked container capacitor used in a dynamic random access memory circuit. The double sided electrode is preferably formed of a conductive metal, provided that an oxide of the metal is conductive. The double sided electrode capacitor provides a capacitor that has high storage capacitance which provides an increased efficiency for a cell without an increase in the size of the cell.

**33 Claims, 20 Drawing Sheets**





US006790725B2

(12) **United States Patent**  
**Coursey**

(10) **Patent No.:** **US 6,790,725 B2**  
(45) **Date of Patent:** **Sep. 14, 2004**

(54) **DOUBLE-SIDED CAPACITOR STRUCTURE  
FOR A SEMICONDUCTOR DEVICE AND A  
METHOD FOR FORMING THE STRUCTURE**

6,159,818 A 12/2000 Durcan et al. .... 438/387

\* cited by examiner

(75) **Inventor:** **Belford T. Coursey, Meridian, ID (US)**

(73) **Assignee:** **Micron Technology, Inc., Boise, ID  
(US)**

(\*) **Notice:** Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 54 days.

(21) **Appl. No.:** **10/150,622**

(22) **Filed:** **May 17, 2002**

(65) **Prior Publication Data**

US 2003/0215998 A1 Nov. 20, 2003

(51) **Int. Cl.<sup>7</sup>** ..... **H01L 21/8242**

(52) **U.S. Cl.** ..... **438/253; 438/254; 438/396**

(58) **Field of Search** ..... **438/3, 238-256,  
438/390-399, 381**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

6,060,355 A \* 5/2000 Batra et al. .... 438/255

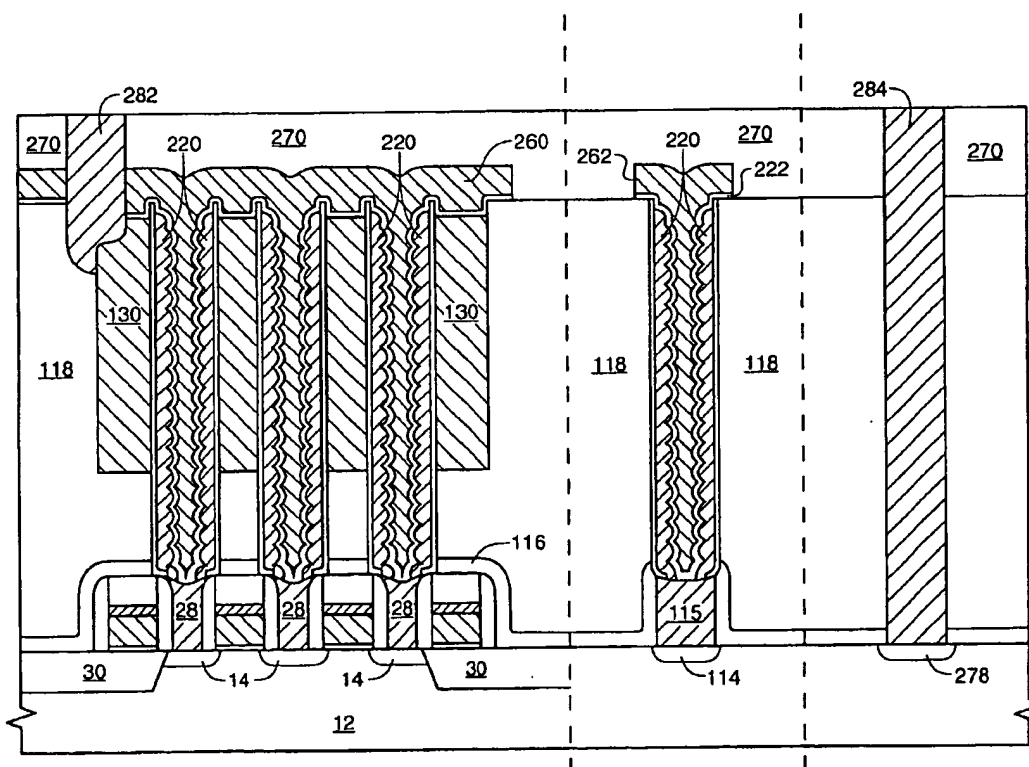
*Primary Examiner*—H. Jey Tsai

(74) *Attorney, Agent, or Firm*—Kevin D. Martin

(57) **ABSTRACT**

A method used to manufacture a semiconductor device comprises providing a first conductive container capacitor top plate layer and etching the first conductive container capacitor top plate layer to form a plurality of openings therein. Subsequently, a container capacitor bottom plate layer is formed within the plurality of openings in the top plate layer such that the bottom plate layer defines a plurality of openings. A second conductive container capacitor top plate layer is formed within the plurality of openings in the bottom plate layer. The first conductive container capacitor top plate layer is electrically coupled with the second conductive container capacitor top plate layer. The first and second conductive container capacitor top plate layers and the container capacitor bottom plate layer form a plurality of container capacitors. A structure resulting from the method is also disclosed.

**20 Claims, 30 Drawing Sheets**











US005792680A

**United States Patent** [19]

Sung et al.

[11] **Patent Number:** 5,792,680[45] **Date of Patent:** Aug. 11, 1998

[54] **METHOD OF FORMING A LOW COST DRAM CELL WITH SELF ALIGNED TWIN TUB CMOS DEVICES AND A PILLAR SHAPED CAPACITOR**

[75] **Inventors:** Janmye Sung, Hsinchu; Chih-Yuan Lu, Hsin Chu; Howard Clayton Kirsch, Taoyuan, all of Taiwan

[73] **Assignee:** Vanguard International Semiconductor Corporation, Hsinchu, Taiwan

[21] **Appl. No.:** 756,129

[22] **Filed:** Nov. 25, 1996

[51] **Int. CL<sup>6</sup>** ..... H01L 21/8238; H01L 21/8242

[52] **U.S. Cl.** ..... 438/210; 438/239; 438/255

[58] **Field of Search** ..... 438/210, 241, 438/238, 239, 255, 381, 398; 257/296, 306, 309

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,435,895	3/1984	Pamillo et al.	29/571
4,525,920	7/1985	Jacobs et al.	29/571
4,707,455	11/1987	Tsang et al.	437/57
4,806,501	2/1989	Baldi et al.	437/67
5,286,991	2/1994	Hui et al.	257/306
5,302,540	4/1994	Ko et al.	437/47

5,336,630	8/1994	Yun et al.	437/52
5,427,974	6/1995	Lur et al.	437/60
5,459,095	10/1995	Huang et al.	437/52
5,547,893	8/1996	Sung	438/210
5,633,181	5/1997	Hayashi	438/210

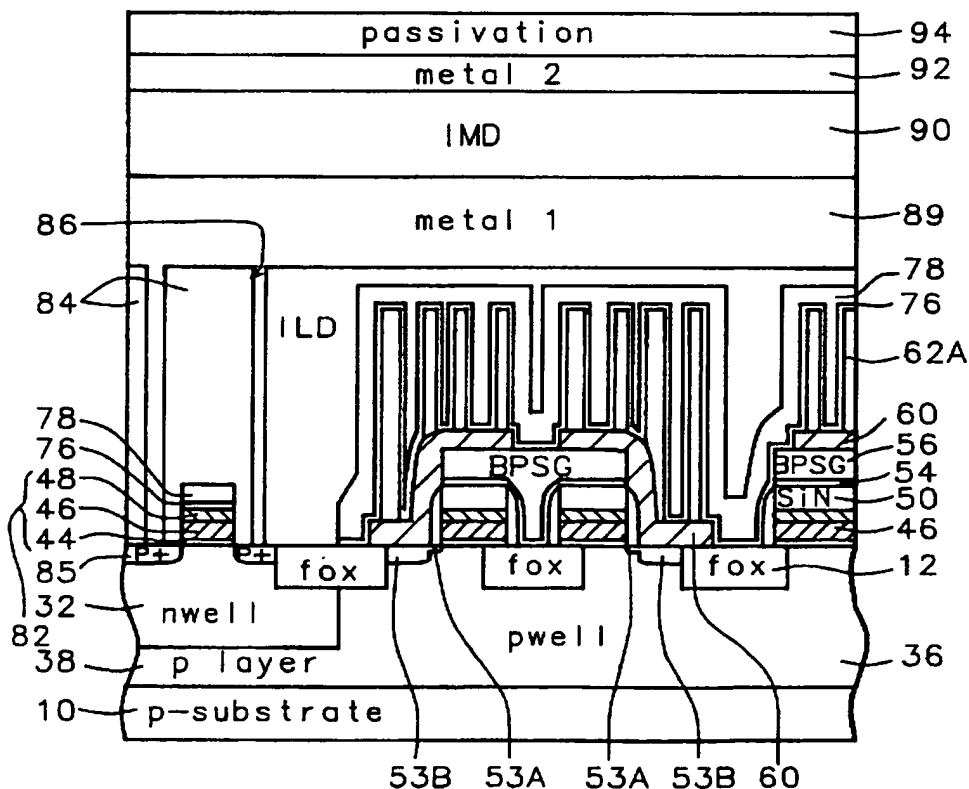
**Primary Examiner**—Joni Chang

**Attorney, Agent, or Firm**—George O. Saile; Stephen B. Ackerman; William J. Stoffel

[57] **ABSTRACT**

The invention is a method of forming a reduced cost DRAM. The process has two embodiments for forming twin wells and two embodiments for forming pillar shaped capacitor electrodes. The twin well embodiments are simple low cost processes. The embodiments for forming the electrode pillars begin by forming a tungsten silicide conductive layer on a first planarization layer. For the first embodiment, the pillars are formed using a photolithography mask with a pattern of spaced transparent areas. The dimensions of the spaced transparent areas and distances between the spaced transparent areas are smaller than the resolution of the lithographic tool. Spaced oxide islands are formed with the mask and are used as an etch mask to form spaced pillars from the conductive layer. This first embodiment for fabricating the multiple pillar capacitor forms pillars of a smaller dimension than the resolution of the photolithography tool. The second embodiment for forming the pillars involves using small titanium silicide islands as an etch mask to define the pillars.

22 Claims, 23 Drawing Sheets





US006037217A

**United States Patent** [19][11] **Patent Number:** **6,037,217****Linliu**[45] **Date of Patent:** **Mar. 14, 2000**

[54] **METHOD OF FABRICATING A CAPACITOR  
ELECTRODE STRUCTURE IN A DYNAMIC  
RANDOM-ACCESS MEMORY DEVICE**

5,918,122 6/1999 Parekh et al. .... 438/253

[75] Inventor: **Kung Linliu, Hsinchu, Taiwan***Primary Examiner—Jey Tsai**Attorney, Agent, or Firm—Thomas, Kayden, Horstemeyer  
& Risley*[73] Assignee: **Worldwide Semiconductor  
Manufacturing Corp., Hsinchu,  
Taiwan**[57] **ABSTRACT**

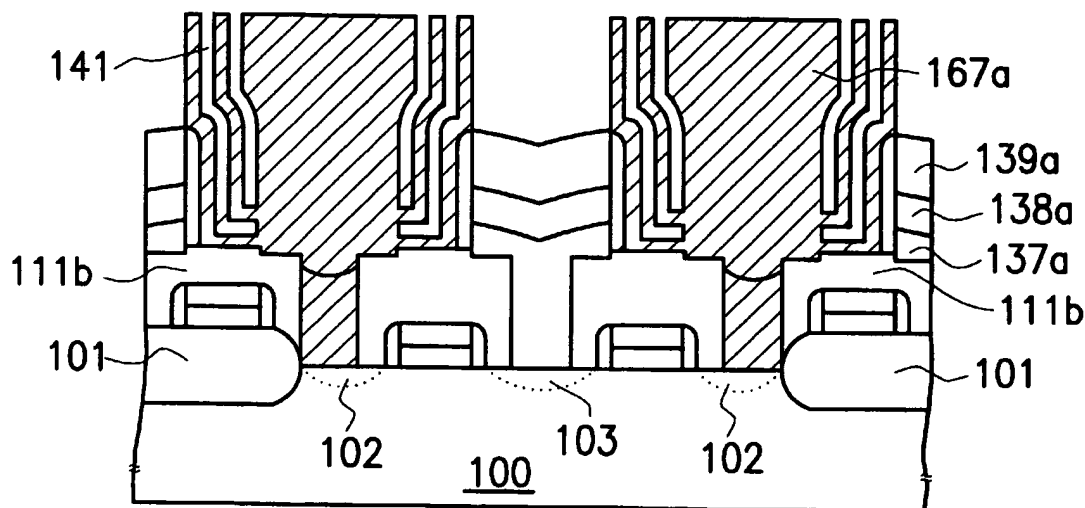
An integrated circuit (IC) fabrication method is provided for the fabrication of an electrode structure having an increased surface area for a double-crown type of capacitor in a dynamic random-access memory (DRAM) device. In this method, damascene technology is used, which can help reduce the height difference between the memory cell region and the peripheral region, thus eliminating the required planarization process in the prior art. Moreover, this method can provide an electrode structure having a large surface area that allows the associated capacitor to be considerably increased in capacitance as compared to the prior art while requiring no increase in the layout area in the integrated circuit.

[21] Appl. No.: **09/250,372**[22] Filed: **Feb. 16, 1999**[30] **Foreign Application Priority Data**

Nov. 16, 1998 [TW] Taiwan ..... 87118920

[51] Int. Cl.<sup>7</sup> ..... **H01L 21/8242**[52] U.S. Cl. .... **438/253; 438/254**[58] Field of Search ..... **438/238–242,  
438/250–256, 381, 393–399**[56] **References Cited****U.S. PATENT DOCUMENTS**

5,874,335 2/1999 Jenq ..... 438/253

**13 Claims, 6 Drawing Sheets**



US006445023B1

(12) **United States Patent**  
**Vaartstra et al.**

(10) **Patent No.:** **US 6,445,023 B1**  
(45) **Date of Patent:** **Sep. 3, 2002**

(54) **MIXED METAL NITRIDE AND BORIDE  
BARRIER LAYERS**

(75) Inventors: **Brian A. Vaartstra**, Nampa; **Donald L. Westmoreland**, Boise, both of ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/268,326**

(22) Filed: **Mar. 16, 1999**

(51) Int. Cl.<sup>7</sup> ..... **H01L 27/108**; **H01L 29/76**;  
**H01L 29/94**; **H01L 31/119**

(52) U.S. Cl. .... **257/295**; **257/306**; **257/308**

(58) Field of Search ..... **257/295-310**;  
**438/253-254**, **396-399**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,142,438 A	8/1992	Reinberg et al.	
5,187,638 A	2/1993	Sandhu et al.	
5,198,386 A	3/1993	Gonzalez	
5,290,588 A *	3/1994	Romero et al.	427/123
5,362,632 A	11/1994	Mathews	
5,406,447 A	4/1995	Miyazaki	
5,464,786 A	11/1995	Figura et al.	
5,478,772 A	12/1995	Fazan	
5,489,548 A *	2/1996	Nishioka et al.	438/396
5,498,562 A	3/1996	Dennison et al.	
5,504,041 A	4/1996	Summerfelt	
5,506,166 A	4/1996	Sandhu et al.	
5,567,964 A	10/1996	Kashihara et al.	
5,568,352 A	10/1996	Hwang	
5,585,300 A	12/1996	Summerfelt	
5,605,857 A	2/1997	Jost et al.	
5,654,222 A	8/1997	Sandhu et al.	
5,654,224 A	8/1997	Figura et al.	
5,663,088 A	9/1997	Sandhu et al.	
5,665,628 A	9/1997	Summerfelt	

5,679,980 A	10/1997	Summerfelt	
5,686,339 A	11/1997	Lee et al.	
5,688,724 A	11/1997	Yoon et al.	
5,690,727 A	11/1997	Azuma et al.	
5,696,018 A	12/1997	Summerfelt et al.	
5,717,250 A	2/1998	Schuele et al.	
5,760,474 A	6/1998	Schuele	
5,933,365 A *	8/1999	Klersy et al.	257/5
6,090,697 A *	7/2000	Xing et al.	

**OTHER PUBLICATIONS**

Matsuhashi et al., *Optimum Electrode Materials for Ta<sub>2</sub>O<sub>5</sub> Capacitors at High and Low Temperature Processes*, Extended Abstract of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 853-855.

Kwon, et al., *Degradation-Free Ta<sub>2</sub>O<sub>5</sub> Capacitor after BPSG Reflow at 850° C for High Density DRAMs*, *IEEE*, 1993, pp. 53-56.

Shappirio, et al., *Diboride Diffusion Barriers in Silicon and GaAs Technology*, *J. Vac. Sci. Technol. B*, vol. 4, No. 6, Nov./Dec. 1986, pp. 1409-1415.

Rebhoiz, et al., *Structure, Mechanical and Tribological Properties of Ti-B-N and Ti-Al-B-N Multiphase Thin Films Produced by Electron-Beam Evaporation*, *J. Vac. Sci. Technol. A* 16(5), Sep./Oct. 1998, pp. 2850-2857.

\* cited by examiner

*Primary Examiner*—Tom Thomas

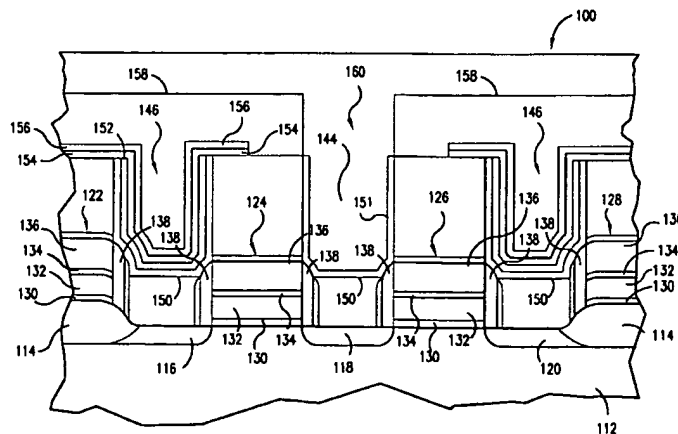
*Assistant Examiner*—Cuong Quang Nguyen

(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin & Oshinsky LLP

(57) **ABSTRACT**

Mixed metal aluminum nitride and boride diffusion barriers and electrodes for integrated circuits, particularly for DRAM cell capacitors. Also provided are methods for CVD deposition of M<sub>x</sub>Al<sub>y</sub>N<sub>z</sub>B<sub>w</sub> alloy diffusion barriers, wherein M is Ti, Zr, Hf, V, Nb, Ta, Cr, Mo, or W; x is greater than zero; y is greater than or equal to zero; the sum of z and w is greater than zero; and wherein when y is zero, z and w are both greater than zero.

**41 Claims, 16 Drawing Sheets**





US006693015B2

(12) **United States Patent**  
Carstensen

(10) Patent No.: **US 6,693,015 B2**  
(45) Date of Patent: **Feb. 17, 2004**

(54) **METHOD FOR IMPROVED PROCESSING  
AND ETCHBACK OF A CONTAINER  
CAPACITOR**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

(75) Inventor: **Robert K. Carstensen, Boise, ID (US)**

5,401,681 A 3/1995 Dennison

5,854,119 A 12/1998 Wu et al.

(73) Assignee: **Micron Technology, Inc., Boise, ID  
(US)**

5,981,989 A \* 11/1999 Miyake ..... 257/296

6,027,984 A 2/2000 Thakur et al.

6,037,213 A 3/2000 Shih et al.

6,042,999 A 3/2000 Lin et al.

6,077,790 A 6/2000 Li et al.

(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 0 days.

\* cited by examiner

(21) Appl. No.: **09/928,308**

(22) Filed: **Aug. 14, 2001**

(65) **Prior Publication Data**

US 2002/0000596 A1 Jan. 3, 2002

*Primary Examiner*—Matthew Smith

*Assistant Examiner*—V. Yevsikov

(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin &  
Oshinsky LLP

**Related U.S. Application Data**

(62) Division of application No. 09/235,752, filed on Jan. 25,  
1999, now Pat. No. 6,319,789.

(51) **Int. Cl.<sup>7</sup>** ..... **H01L 21/336**

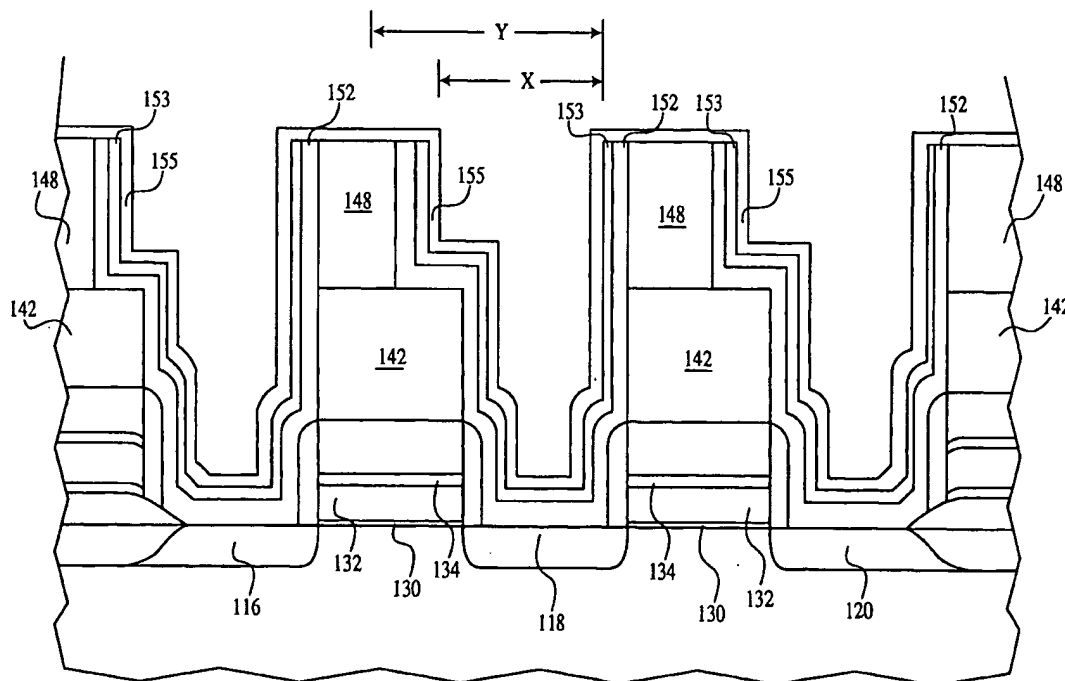
(52) **U.S. Cl.** ..... **438/306; 438/296; 438/301;**  
**438/303; 438/310; 438/532; 438/396; 438/239;**  
**438/242; 438/253; 438/387**

(58) **Field of Search** ..... **257/296, 301,**  
**257/303, 306-310, 532; 438/396, 239, 242,**  
**253, 387**

(57) **ABSTRACT**

A capacitor having improved size for enhanced capacitance and a method of forming the same are disclosed. In one embodiment, the capacitor is a stacked container capacitor used in a dynamic random access memory circuit. The capacitor provides a capacitor that has high storage capacitance which provides an increased efficiency for a cell without an increase in the size of the cell.

**38 Claims, 17 Drawing Sheets**





US006696336B2

(12) **United States Patent**  
**DeBoer et al.**

(10) **Patent No.:** **US 6,696,336 B2**  
(45) **Date of Patent:** **Feb. 24, 2004**

(54) **DOUBLE SIDED CONTAINER PROCESS  
USED DURING THE MANUFACTURE OF A  
SEMICONDUCTOR DEVICE**

(75) **Inventors:** **Scott J. DeBoer, Boise, ID (US);  
Ronald A. Welmer, Boise, ID (US);  
John T. Moore, Boise, ID (US)**

(73) **Assignee:** **Micron Technology, Inc., Boise, ID  
(US)**

(\*) **Notice:** Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** **09/855,217**

(22) **Filed:** **May 14, 2001**

(65) **Prior Publication Data**

US 2002/0168830 A1 Nov. 14, 2002

(51) **Int. Cl.<sup>7</sup>** ..... **H01L 21/8242; H01L 21/20**

(52) **U.S. Cl.** ..... **438/253; 438/254; 438/396;  
438/397**

(58) **Field of Search** ..... **438/210, 239,  
438/253, 254, 396, 397**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

4,656,732 A	4/1987	Teng et al.	438/639
5,144,579 A *	9/1992	Okabe et al.	365/149
5,338,700 A	8/1994	Dennison et al.	437/60
5,401,681 A	3/1995	Dennison	437/60
5,834,845 A	11/1998	Stolmeijer	257/752
5,843,830 A	12/1998	Graettinger et al.	438/396
5,844,771 A	12/1998	Graettinger et al.	361/303
5,869,861 A	2/1999	Chen	257/306
5,956,594 A	9/1999	Yang et al.	438/396
5,989,952 A	11/1999	Jen et al.	438/253
6,046,093 A	4/2000	DeBoer et al.	438/396
6,100,137 A	8/2000	Chen et al.	438/253
6,127,260 A	10/2000	Huang	438/253
6,134,137 A *	10/2000	Kurth et al.	365/149
6,140,172 A	10/2000	Parekh	438/238

6,168,984 B1	1/2001	Yoo et al.	438/244
6,187,624 B1	2/2001	Huang	438/253
6,221,711 B1	4/2001	Roberts et al.	438/253
6,251,726 B1	6/2001	Huang	438/253
6,300,191 B1	10/2001	Yu et al.	438/253

**OTHER PUBLICATIONS**

Related application entitled: Reduced Aspect Ratio Digit  
Line Contact Process Flow Used During the Formation of a  
Semiconductor Device by Brent A. McClure, Micron Tech-  
nology, Inc., Ser. No. 09/765,885, filed Jan. 16, 2001.

U.S. patent application: "Double Sided Container Capacitor  
For DRAM Cell Array And Method Of Forming Same," Ser.  
No. 09/569,570, Sanh D. Tang and Robert J. Burke Inven-  
tors, commonly assigned to Micron Technology, Inc.

\* cited by examiner

*Primary Examiner*—Amir Zarabian

*Assistant Examiner*—Pamela Perkins

(74) *Attorney, Agent, or Firm*—Kevin D. Martin

(57) **ABSTRACT**

A method used during the formation of a semiconductor  
device comprises providing a wafer substrate assembly  
comprising a plurality of digit line plug contact pads and  
capacitor storage cell contact pads which contact a semi-  
conductor wafer. A dielectric layer is provided over the  
wafer substrate assembly and etched to expose the digit line  
plug contact pads, and a liner is provided in the opening. A  
portion of the digit line plug is formed, then the dielectric  
layer is etched again to expose the capacitor storage cell  
contact pads. A capacitor bottom plate is formed to contact  
the storage cell contact pads, then the dielectric layer is  
etched a third time using the liner and the bottom plate as an  
etch stop layer. A capacitor cell dielectric layer and capacitor  
top plate is formed which provides a double-sided container  
cell. An additional dielectric layer is formed, then the  
additional dielectric layer, cell top plate, and the cell dielec-  
tric are etched to expose the digit line plug portion. Finally,  
a second digit line plug portion is formed to contact the first  
plug portion. A novel structure resulting from the inventive  
method is also discussed.

**20 Claims, 10 Drawing Sheets**

